TDB-ACC-NO: NN9508185

DISCLOSURE TITLE: Universal Asynchronous Receiver-Transmitter Chip with Switchable Clock Rate

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, August 1995, US

VOLUME NUMBER: 38

ISSUE NUMBER: 8

PAGE NUMBER: 185 - 186

PUBLICATION-DATE: August 1, 1995 (19950801)

CROSS REFERENCE: 0018-8689-38-8-185

DISCLOSURE TEXT:

Disclosed is method for operating a Universal Asynchronous Receiver-Transmitter (UART) chip at a first clock frequency for handling relatively low serial data rates and at one or more higher frequencies for handling relatively high serial data rates. While the standard UART clock rate of 1.8432 MHz (megahertz) provides the best support for standard data rates, such as 300, 1200, and 9600 baud, about 38.4 kbaud (kilobaud) is the highest rate which can be comfortably supported at this clock rate. Thus, this clock frequency does not allow the use of higher data rates, particularly in the range of 56 kbaud to 512 kbaud.

In the implementation of this method, the highest baud rate accurately supported at the standard UART frequency, such as 38.4 kbaud at 1.8432 MHz, is first determined.

Next, the clock frequency which provides the greatest accuracy for the highest baud rate supported by the hardware is determined. For example, for a conventional implementation, this frequency is 8 MHz. In the system, the Basic Input/Output System (BIOS) level code is provided with a capability to recognize the baud rate requested by a user. This code is also provided with a capability for manipulating the UART directly to make clock frequency changes. Preferably, a data structure is provided which remembers the last frequency at which the clock rate of the UART was set, eliminating a need to read the clock setting every time it is needed. The code used to change the clock frequency is preferably placed in a module which is separate from the code used to perform the actual changes.

During operation of the system with this method, if the baud rate of a communication request matches the range best supported by the presently used clock frequency, the communication request is passed to the UART chip in the conventional manner. If the requested baud rate is higher than the maximum supported by the hardware, the clock frequency and baud rate are set to their maximum levels, and a "not supported" code is sent if possible. Otherwise, the requested baud rate is supported, but the clock needs to be set for the optimum frequency. Changing the clock rate may require saving the contests of several registers in the UART chip, modifying the contents of other such registers, and restoring the saved contents.

An appropriate frequency divisor is set in the UART to achieve the correct frequency.

While this method has been particularly described in a form using two clock frequencies, it may be extended to use three or more clock frequencies, each of which provides optimal support for a range of data rates.